AI/ML-Driven VLSI Design Optimization:

Machine Learning for Circuit Layout Optimization

Report submitted to GITAM (Deemed to be University) as a partial fulfillment of the requirements for the award of the Degree of Bachelor of Technology in (Electrical, Electronics and Communication Engineering)



DEPARTMENT OF ELECTRICAL, ELECTRONICS AND COMMUNICATION ENGINEERING

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**DECLARATION**

I/We declare that the project work contained in this report is original and it has been done by me under the guidance of my project guide.

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**CERTIFICATE**

This is to certify that Jerripothula Keerthy bearing BU22EECE0100251 has satisfactorily completed Mini Project Entitled in partial fulfillment of the requirements as prescribed by University for VIIth semester, Bachelor of Technology in “Electrical, Electronics and Communication Engineering” and submitted this report during the academic year 2025-2026.

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**Chapter 1: Introduction**

* 1. Overview of the problem statement

The thesis investigates the application of artificial intelligence and machine learning techniques to optimize Very Large Scale Integration (VLSI) circuit design, with a specific focus on automated placement and routing optimization. As semiconductor technology continues to advance toward smaller nodes and higher transistor densities, traditional design methodologies face increasing challenges in achieving optimal power, performance, and area (PPA) metrics while maintaining signal integrity

* 1. Objectives and goals

This thesis aims to achieve the following specific objectives:

**1. Develop AI-Enhanced Optimization Algorithms**: Create machine learning-based algorithms for automated VLSI placement and routing optimization, focusing on genetic algorithms and reinforcement learning approaches.

**2. Multi-Objective Optimization Framework:** Implement a comprehensive framework that simultaneously optimizes power consumption, performance, area efficiency, and signal integrity.

**3. Experimental Validation:** Conduct extensive experimental evaluation using industry standard benchmarks to demonstrate the effectiveness of the proposed approaches.

**4. Comparative Analysis:** Perform detailed comparison with traditional optimization methods to quantify improvements and identify application domains where AI techniques provide maximum benefit. 5. Implementation Recommendations: Provide practical guidelines for integrating AI-driven optimization techniques into existing VLSI design flows.

**Goals:**

* Develop AI-enhanced optimization algorithms for automated VLSI placement and routing.
* Implement a comprehensive framework that simultaneously optimizes power consumption, performance, area efficiency, and signal integrity.
* Demonstrate the effectiveness of the proposed approach through experimental validation using industry-standard benchmarks.

**Chapter 2 : Literature Review**

|  |  |  |  |
| --- | --- | --- | --- |
| TITLE & AUTHOR | METHODOLOGY | RESULT | PROBLEM STATEMENT |
| “Power Estimation of Digital VLSI Circuits Using Machine Learning”  Manish I. Patel And Srushti Patel  2024 | Circuits were designed in verilog, features collected using Quartus , power measured using powerplay, a dataset was made.  **ML Models used:** four ML models (Tree Regression, Gaussian Process, SVM, Ensemble) were trained in MATLAB With 5-fold crossvalidation **Comparison Metrics:** R² (accuracy) and RMSE (error). | Tree Regression performed best.   * Achieved R² ≈   0.98 (very high accuracy) and RMSE ≈ 0.296  (low error).  Proved that ML models can predict power much faster than traditional simulations . | * At higher abstraction levels → fast but less accurate. * At lower abstraction levels → accurate but very slow and time- consuming. * As designs grow bigger, these simulation methods become too slow and computationally expensive. |
| “Machine Learning Based Power Estimation for CMOS VLSI Circuits” V . Govindaraj and  B. Arunadevi  2021 | Training and testing performed on the ISCAS’89 benchmark dataset. The data was normalized and used to train BPNN and RF models. RF was tuned with 10-fold cross- validation and further optimized using NSGA- II. **Comparison Metrics:** RF and BPNN were compared using Error %, MSE, RMSE, and R. | Random Forest achieved very accurate predictions (Error 1.4%–  6.8%, MSE =  1.46E-06, RMSE  = 0.000116, R = 0.99938) and  clearly outperformed BPNN. | * Neural networks like BPNN also need large data and more computation time. * A faster, simpler, and accurate method is needed. |
| “Power Consumption Prediction of Digital Circuits using Machine Learning”  Modi Divy Bhavesh; Nair Anoopkumar Anilkumar; Dipesh Panchal; Manish I. Patel; Ruchi Gajjar  2022 | Built dataset from small circuits (PMOS RLI, NMOS RLI, CMOS NAND  gate).**ML Models:** Linear, Polynomial, Decision Tree, Random Forest , Extra Tree.  **Training & Testing:** Divided data into training and testing sets.  **Evaluated models** using R², and MSE. | For RLI circuits, Extra Tree perform best.  For NAND  circuits, Polynomial Regression perform best. Overall, ML models predicted power  accurately and faster than traditional simulations. | * As circuits grow larger, these methods become impractical. * A faster and reliable method is needed. |
| “Power Estimation of Synchronous Sequential VLSI Circuits Using Boosting Techniques”  Givari Santhosh, Ajay Singh Raghuvanshi  2023 | Used three machine learning algorithms – AdaBoost, Gradient Boosting, and Extreme Gradient Boosting – on ISCAS’89 benchmark circuits. Data was normalized and parameters optimized using Grid Search & Random Search to improve accuracy.  **Comparison Metrics:**  MSE, RMSE and R score. | Gradient Boosting with Grid Search performed best (R = 0.99746, RMSE = 3.143e-  5). It accurately predicts power, reducing the need for time- consuming simulations. | * Traditional SPICE simulations for power estimation are slow and costly. As chips get complex, early power prediction becomes essential to avoid chip damage and speed up design |
| Power Prediction of VLSI Circuits Using Machine Learning **Authors**: E. Poovannan, S. Karthik | Developed a ML-CPE (Machine Learning-based Circuit Power Estimation) using regression models: Linear Least Squares, Ridge, K-Nearest Neighbors, and Multi- Layer Perceptron. Utilized CNN architecture for feature extraction from netlists and simulation logs. Simulated ISCAS’89 benchmarks and used SPEF data for parasitic modeling. | Achieved prediction accuracy with error rates below 6%. Reduced simulation time from hours to milliseconds.  Demonstrated scalability across filter sizes and circuit types. Validated performance using training/testing datasets and  error analysis. | * VLSI power estimation during testing is slow and costly. * Full test vector simulation is impractical. * Worst-case power scenarios may be missed. * A predictive method is needed to spot high-power tests efficiently. |
| **GLAAPE: Graph Learning Assisted Average Power Estimation for Gate- level Combinational Designs** — Rakesh M B, Sai Pranav K R, Pabitra Das, Amit Acharyya — Department of Electrical Engineering, IIT Hyderabad — IEEE ICECS 2022 | Converts gate-level netlists into graph structures using Networkx and DGL. Assigns node features (static probabilities, switching probabilities, inversion flags) and edge features (16 transition correlation coefficients + 1 state correlation coefficient).  Uses an inductive GNN architecture with modified message passing and GCN aggregator. Trains on toggle rates from gate- level SAIF files; tests using RTL SAIF input toggle rates. Architecture: FC1 (4→128), GNN Layer, FC2 (128→16),  FC3 (16→4 with softmax). | Average power estimation accuracy: GLAAPE 95.63%,  outperforming GRANNITE (92.35%) and CRPET (70.35%).  Toggle rate prediction accuracy: GLAAPE 83.43%, vs GRANNITE 69.48%.  Inference throughput: GLAAPE 2.04  kHz, 15.69×  faster than CGPET (0.13  kHz). Transferability: 13.95%  improvement over GRANNITE in predicting  unseen logic cells. | * Existing power estimation methods trade off between accuracy (gate-level) and speed (RTL), while ML models lack transferability and need retraining for new designs. * A fast, accurate, and transferable solution is needed GLAAPE addresses this by learning toggle rate propagation using inductive GNNs. |
| The Meritorious Effects of Machine Learning Algorithms in Assessment of Power Consumption by Arithmetic Circuits in IC Design  **Authors:** Saravanakumar C, Sasikala A, Sivanantham P, Syed Nasruddin S, Sowmiya P, Subhashini N | Six machine learning algorithms (Constant Model, Linear Regression, Neural Networks, kNN, SVM, AdaBoost) were trained on ISCAS'89 benchmark circuits using Orange Data Mining Tool. Input features included number of gates, PIs, POs, logic types.  Performance was evaluated using RMSE, MAE, and R² metrics | AdaBoost achieved the lowest RMSE (0.006), showing superior performance compared to other models.  The constant model performed worst, making it unsuitable. The study demonstrates that ML-based powerestimation is feasible  without prior knowledge of circuit connections. | **1. Limitations of Traditional Methods:**  Power estimation is slow, resource-heavy, and needs detailed circuit knowledge.  **2. Need for Advancement:**  A faster, accurate, and data-driven method is required for early-stage power estimation. |
| High-Level Early Power Estimation of FPGA IP Based on Machine Learning  AUTHORS:  Majdi Richa, Jean- Christophe Prévotet, Mickaël Dardaillon (Univ Rennes, INSA Rennes, CNRS, IETR),  Mohamad Mroué, Abed Ellatif Samhat (Lebanese University) | Developed a fully automated measurement system (ACDGAS) to collect real power data, then trained a supervised ANN using control signals (CS), Switching Rate (SR), and Percentage Level High (PLH). The neural network model was implemented in TensorFlow/Keras, trained with 80-20 split, optimizedusing Adam and SeLU activation | Achieved <1% Mean Absolute Percentage Error (MAPE) for average power estimation on FPGA IP circuits (Xilinx Artix-7).  Showed scalability and suitability for early-stage power prediction, potentially enabling runtime power management with DVFS in the  future | * Early-stage FPGA power estimation is challenging. * Tight power budgets increase the difficulty. * Existing methods are either slow (low-level sims) or inaccurate (simplified models). * This leads to unreliable power predictions. |
| GLAAPE: Graph Learning Assisted Average Power Estimation for Gate- level Combinational Designs AUTHORS:  Rakesh M B, Sai Pranav K R, Pabitra Das, Amit Acharyya (IIT Hyderabad) | Proposed GLAAPE, an inductive Graph Neural Network (GNN)-based model that learns toggle rate propagation using node and edge features extracted from netlist graphs. Trained with gate- level SAIF file data (ground truth) and tested on unseen circuits using RTL simulation input toggle rates | Achieved 95.63% average power estimation accuracy, outperforming commercial RTL tools (CRPET) by 25.28% and GRANNITE by 3.28%.  Inference throughput was  15.69× faster than commercial gate-level tools (CGPET),  proving  GLAAPE’s  efficiency and transferability | * Gate-level power estimation is accurate but slow. * RTL-based estimation is faster but less accurate. * Need for a fast, accurate, and generalizable power estimation method. * Should work well on unseen circuits. |

**Chapter 3 : Strategic Analysis and Problem Definition**

* 1. SWOT Analysis

**Strengths**

* **Hybrid Framework:** The project uses a novel hybrid framework that combines the global exploration of genetic algorithms (GA) with the policy-based refinement of reinforcement learning (RL).
* **Multi-Objective Optimization:** The framework is designed to simultaneously optimize multiple, often conflicting, objectives such as power consumption, performance, area utilization, and signal integrity.
* **Significant Performance Gains:** The proposed approach demonstrates substantial improvements over conventional methods. It achieves a 25% power consumption reduction , a 35x performance speedup in routing , and a 41% enhancement in signal integrity metrics.
* **Scalability and Robustness:** The research validates the approach's effectiveness on industrial-scale designs with over 10 million components maintaining solution quality and demonstrating sub-quadratic runtime scaling.

**Weaknesses**

* **High Computational Requirements:** The AI-driven approach requires more computational resources than traditional methods, particularly during the initial learning phases.
* **Algorithm Complexity:** The hybrid GA-RL framework is inherently more complex than traditional approaches, requiring specialized expertise for effective deployment and troubleshooting.
* **Interpretability Issues:** The "black-box" nature of some machine learning components can make it difficult for designers to understand why certain optimization decisions were made, which could limit acceptance in environments where transparency is critical.

**Opportunities**

* **Industry Adoption:** The research provides a foundation and practical guidelines for integrating AI-driven optimization into existing VLSI design flows.
* **Expanded Application:** The success of this approach suggests it could be adapted for other engineering domains with similar multi-objective challenges, such as **analog and mixed-signal circuits**.
* **Transfer Learning:** Future work can investigate how to transfer optimization knowledge between similar design problems to reduce training time for new projects.
* **Enhanced Interpretability:** There is an opportunity to develop explainable AI (XAI) techniques to provide designers with insights into optimization decisions, which would improve trust and enable manual refinement.

**Threats**

* **Industry Validation:** The semiconductor industry has stringent quality requirements that necessitate extensive validation of AI-optimized designs, which may initially slow adoption until confidence is established.
* **Intellectual Property Concerns:** Companies may be hesitant to share the proprietary design data needed to train machine learning models.
* **Competition:** The field of AI/ML in EDA is highly competitive, with other state-of-the-art academic methods and commercial tools constantly being developed.
  1. Project Plan - GANTT Chart

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TASK/TIME | AUGUST 2025 | SEPTEMBER 2025 | OCTOBER 2025 | NOVEMBER 2025 | DECEMBER 2025 | JANUARY 2026 | FENRUARY 2026 | MARCH 2026 | APRIL 2026 |
| PROJECT SELECTION |  |  |  |  |  |  |  |  |  |
| IDENTIFICATION OF PROBLEM |  |  |  |  |  |  |  |  |  |
| LITERATIVE SURVEY |  |  |  |  |  |  |  |  |  |
| IDENTIFICATION TOOLS/ALGORITHMS |  |  |  |  |  |  |  |  |  |
| MODEL DESIGN |  |  |  |  |  |  |  |  |  |
| MODEL IMPLEMENTATION |  |  |  |  |  |  |  |  |  |
| SYSTEM DESIGN |  |  |  |  |  |  |  |  |  |
| SYSTEM DEPLOYMENT |  |  |  |  |  |  |  |  |  |

* 1. Problem statement

The primary challenges addressed in this research include:

**1. Complexity Management**: Modern VLSI designs involve millions of design variables and constraints, creating optimization problems of unprecedented complexity that exceed the capabilities of traditional heuristic approaches.

**2. Multi-Objective Optimization:** Achieving optimal trade-offs between conflicting objectives such as power consumption, performance, area utilization, and signal integrity requires sophisticated optimization techniques.

**3. Design Time Constraints**: Increasing market pressures demand shorter design cycles while maintaining or improving quality metrics, necessitating more efficient optimization methodologies.

**4. Technology Scaling Challenges:** As semiconductor technology scales to smaller nodes, new physical effects and design constraints emerge that traditional tools struggle to handle effectively.

**Chapter 4 : Methodology**

* 1. Description of the approach

The methodology used in this research is a **hybrid GA-RL framework** that combines genetic algorithms with reinforcement learning. The framework is designed to leverage the strengths of both techniques to solve the complex, multi-objective VLSI layout optimization problem.

* The **genetic algorithm (GA)** component provides diverse solution exploration. It encodes potential solutions as chromosomes, with genes representing placement and routing configurations. The GA uses a weighted fitness function to evaluate solutions based on optimization objectives and applies genetic operators like selection, crossover, and mutation to evolve a population of solutions.
* The **reinforcement learning (RL)** component enables the fine-tuning of promising solutions and adaptive learning. The RL approach models the optimization as a Markov Decision Process (MDP) and uses a neural network policy to map states to actions. An RL agent learns to optimize its policy to maximize the expected cumulative reward, which is based on improvements in optimization objectives.
* The hybrid approach follows an iterative process: an initial population is generated by the GA. In each generation, the fitness of all solutions is evaluated. The RL policy then refines the top-performing solutions, and the GA applies selection, crossover, and mutation to create the next generation. Finally, the RL policy is updated based on the improvements observed during this process.
  1. Tools and techniques utilized
* The implementation of the hybrid GA-RL framework utilized a range of tools and techniques across different domains.
* **Software Languages**: The core algorithm development was done primarily in Python. For performance-critical components, C++ was used to handle large-scale evaluations.
* **Machine Learning Frameworks**: TensorFlow and PyTorch were the deep learning frameworks of choice for implementing the RL policy networks.
* **Libraries and Tools**: NetworkX was used for graph processing to represent netlists. For visualization and analysis, the researchers used Matplotlib and Plotly.
* **Algorithm Implementations**: The GA component used specialized operators for VLSI optimization, including chromosome encoding for placement and routing , tournament selection , and problem-specific crossover and mutation operators. The RL component employed a deep Q-network (DQN) approach with experience replay.
  1. Design considerations

The research paper outlines several critical design considerations to address the complexities of VLSI optimization.

* **Multi-Objective Optimization**: The framework addresses the need to simultaneously optimize conflicting objectives like power consumption, performance, area utilization, and signal integrity. It employs a Pareto optimization strategy to maintain a set of non-dominated solutions, and it dynamic weighting and solution ranking to guide the selection process.
* **Scalability**: The system is designed to handle large-scale designs with millions of components. The framework uses several parallelization strategies, such as parallel fitness computation and distributed RL training, to improve runtime performance. It also employs efficient memory management techniques like lazy evaluation and hierarchical data structures.
* **Implementation Architecture**: The system is built with a modular architecture consisting of interconnected components. These components include a design parser, an optimization engine, an evaluation module, a solution generator, and a verification module. This modularity allows for extensibility and integration with existing design flows.
* **Experimental Validation**: The research uses industry-standard benchmarks and custom test cases to ensure the effectiveness of the proposed approach. The performance is measured using a comprehensive set of metrics, including power consumption, area efficiency, and signal integrity. The hybrid approach is compared against traditional methods, commercial tools, and pure GA and RL implementations to quantify its improvements.

**Chapter 5 : Implementation**

* 1. Description of how the project was executed
  2. Challenges faced and solutions implemented

**Chapter 6: Results**

* 1. outcomes
  2. Interpretation of results
  3. Comparison with existing literature or technologies

**Chapter 7: Conclusion**

**Chapter 8 : Future Work**

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